Statistical Analysis Report
(DFSS Approach)

on

PLCC Surface Mount Socket

Soldering Socket Leads to Board Pads

by

David C. Wilson, MSEE
Wilson Consulting Services, LLC
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Objective:

To determine probability of a socket pin lead being unsoldered and/or a poor solder connection to the pad on the printed circuit board.

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Date: October 23, 2002

Subject: Possible affected socket numbers: 39000SM, 39001SM, and 39002SM

Issue: Field failures due to unsoldered or poor solder connection of the pin leads for the surface mounted sockets. This report addresses the gap distance only and does not make any attempt with probabilities relative to lead contamination, etc.

Requirement: On the basis of the current manufacturing process**,** the distance between the contact tail and pad on the PC board must not exceed 0.006 inch in order to ensure a good solder connection.

Illustration

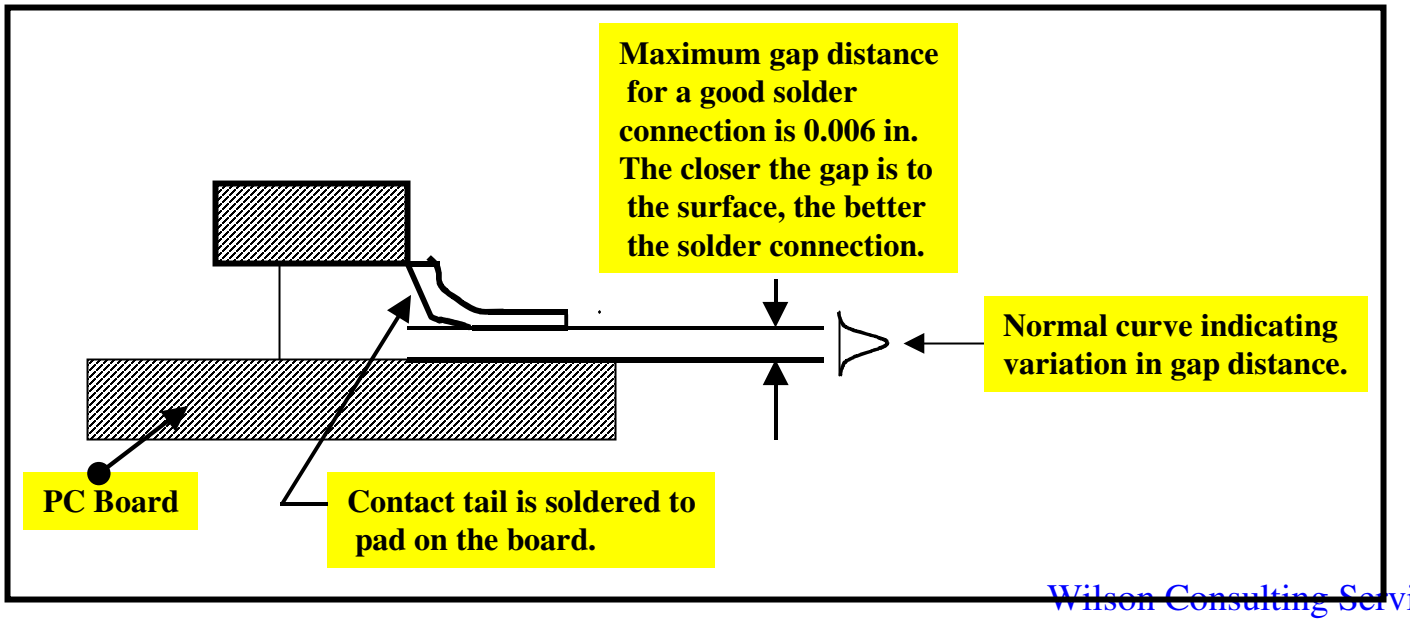

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Figure 1

Variation is inherently in any process:

In an attempt to quantify the problem without much information on the underlying failure distribution, Monte Carlo simulation was employed to predict the magnitude of the problem.

Assumptions:

- Variation in distance or gap is normally distributed
- Three sigma process
- Three scenarios
  - Distance (Gap) centered at mean = 0.003 in.
  - Distance (Gap) is off center at mean = 0.004 in.
  - Distance (Gap) is off center at mean = 0.002 in.

***Important note:* All statistical analyses are reasonable estimates based on an assumption of normality for both the gap distance and manufacturing process whether the gap distance is centered or shifted away from center.**

Analysis methods*

- Without Monte Carlo Simulation
- Monte Carlo Simulation
- Chi-Square Test
- **Comments**

*The two methods shown in long-hand calculations in this report were performed using mean = 0.003, centered, with a standard deviation of 0.001 inch. All scenarios followed the same rule, but it was not necessary to show detail calculations in every case.

Summary

Refer to tables 1 and 2

Analysis 1. The probability of the gap being greater than 0.006 inch is 0.135%.

Analysis 2. The probability of the gap being greater than 0.006 in using the Monte Carlo Simulation is 0.145%

Analysis 3. The probability of the gap exceeding 0.006 inch is 2.28%.

Analysis 4. The probability of the gap being greater than 0.006 in using the Monte Carlo Simulation is 1.58%

Analysis 5. The probability of the gap exceeding 0.006 inch is 0.0032%.

Analysis 4. The probability of the gap being greater than 0.006 in using the Monte Carlo Simulation is 0.0029%.

This table is based on normality of the normal curve shifting in a three sigma process.

Scorecard

Product: Prediction Analysis for Soldering Process for Socket Leads

Description	Methods	Lower Spec Limit	Upper Spec Limit	Mean	Standard Deviation	Cp	Cpk	ST LT	DPU	Sigma Level Z_{ST}
Assume mean is centered at 0.003 in a 3-simga process with upper gap spec limit = 0.006										
Analysis#1	Without Monte Carlo		0.006	0.003000	0.001000	1.00	1.00	LT	1.350E-03	4.50
Analysis #2	Monte Carlo		0.006	0.003007	0.001005	1.00	0.99	LT	1.450E-03	4.48
Assume mean is off center at 0.004 in a 3-simga process with upper gap spec limit = 0.006										
Analysis#3	Without Monte Carlo		0.006	0.004	0.001	1.00	0.67	LT	2.275E-02	3.50
Analysis #4	Monte Carlo		0.006	0.004	0.00093	1.08	0.72	LT	1.576E-02	3.65
Assume mean is off center at 0.002 in a 3-simga process with upper gap spec limit = 0.006										
Analysis#5	Without Monte Carlo		0.006	0.0020	0.001	1.00	0.67	LT	3.179E-05	5.50
Analysis #6	Monte Carlo		0.006	0.00198	0.000998	1.00	0.66	LT	2.823E-05	5.53

Table 1

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The table below is based on the probability of unsoldered pins per 100 boards.

Table 2

Summary Table

	Mean = 0.003			Mean = 0.004			Mean = 0.002		
Methods	Count*	Probabilities	Zst	Count*	Probabilities	Zst	Count*	Probabilities	Zst
Without Monte Carlo	25	0.14%	4.49	409	2.27%	3.50	3	0.0028%	5.07
With Monte Carlo	28	0.16%	4.46	285	1.58%	3.65	3	0.0018%	5.07

***Count = number of unsoldered pins or poor connected pins per 100 boards.**

At the 5% level of significance, the difference between not using Monte Carlo and using Monte Carlo method is statistically significant for mean = 0.003 and mean =0.004. *Hence: p-value = 0.00 < 0.05*. However, when the mean =0.002, both methods offer the best scenarios with the difference being statistically insignificant with a process capability Zst greater than 5.0. *Hence: p-value max. =1.00 > 0.05*.

The Chi-square test was performed to test for independence between the two approaches. Basically, the null hypothesis stated that the approach without Monte Carlo and with Monte Carlo is independent. Therefore, the chi-square test for none or poor solder connections showed evidence of independence with a *p-value = 0.228 > 0.05*.This statistical test essentially confirmed that the Monte Carlo simulation was a reasonable approach to the analysis.

(summary continued)

Analysis 1: Assume mean is centered without Monte Carlo Simulation

Scorecard: Method - Without Monte Carlo Simulation

Conditions: Assume mean is centered at 0.003 in a 3-simga process with

upper gap spec limit = 0.006
Note: Mean is approximated by 1/2*(Max - Min)
Probability of the number of unsoldered and/or poor lead connections for every 100 boards.

Line	P/N	Boards using socket	Type	Defective	# of pins/100 bds.	DPMO	Upper Bound (dpmo)	Z_{ST}
1	3900SM	19	52	7	5200	1346	2527	4.50
2	39001SM	34	44	6	4400	1364	2690	4.50
3	39002SM	36	84	12	8400	1429	2314	4.48

Opportunities	3
TDU	4.138E-03
dpmo	1379
Zst	4.49

Table 3

Note: The column heading "boards using sockets" means the number of different board part numbers using socket type.

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(summary continued)

Analysis 2: Assumed mean is centered using Monte Carlo Simulation

Scorecard: Method - Monte Carlo Simulation

Conditions: Assume mean is centered at 0.003 in a 3-simga process with upper gap spec limit = 0.006

Note: Mean is approximated by 1/2*(Max - Min)

Probability of the number of unsoldered and/or poor lead connections for every 100 boards.

Line	P/N	# of Boards using socket	Socket Type	Defective	# of pins/100 bds.	DPMO	95% Upper Bound (dpmo)	Z_{ST}
1	3900SM	19	52	8	5200	1538	2774	4.46
2	39001SM	34	44	7	4400	1591	2986	4.45
3	39002SM	36	84	13	8400	1548	2459	4.46

Opportunities	3
TDU	4.677E-03
dpmo	1559
Zst	4.46

Table 4

(summary continued)

Analysis 3: Assume mean is off centered without Monte Carlo Simulation

Scorecard: Method - Without Monte Carlo Simulation

Conditions: Assume mean is off centered at 0.004 in a 3-simga process with upper gap spec limit = 0.006
Note: Mean is approximated by 2/3*(Max - Min)
Probability of the number of unsoldered and/or poor lead connections for every 100 boards.

Line	P/N	# of Boards using socket	Socket Type	Defective	# of pins/100 bds.	DPMO	95% Upper Bound (dpmo)	Z_{ST}
1	3900SM	19	52	118	5200	22692	26391	3.50
2	39001SM	34	44	100	4400	22727	26781	3.50
3	39002SM	36	84	191	8400	22738	25599	3.50

Opportunities	3
TDU	6.816E-02
dpmo	22719
Zst	3.50

Table 5

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Analysis 4: Assumed mean is off centered with Monte Carlo Simulation

Scorecard: Method - Monte Carlo Simulation

Conditions: Assume mean is off centered at 0.004 in a 3-simga process with upper gap spec limit = 0.006

Note: Mean is approximated by 2/3*(Max - Min)

Probability of the number of unsoldered and/or poor lead connections for every 100 boards.

Line	P/N	# of Boards using socket	Socket Type	Defective	# of pins/100 bds.	DPMO	95% Upper Bound (dpmo)	Z_{ST}
1	3900SM	19	52	82	5200	15769	18918	3.65
2	39001SM	34	44	70	4400	15909	19376	3.65
3	39002SM	36	84	133	8400	15833	18262	3.65

Opportunities	3
TDU	4.751E-02
dpmo	15837
Zst	3.65

Table 6

Analysis 5: Assumed mean is off centered without Monte Carlo Simulation

Scorecard: Method - without Monte Carlo Simulation

Conditions: Assume mean is off centered at 0.002 in a 3-simga process with upper gap spec limit = 0.006
Note: Mean is approximated by 1/3*(Max - Min)
Probability of the number of unsoldered and/or poor lead connections for every 100 boards.

Line	P/N	# of Boards using socket	Socket Type	Defective	# of pins/100 bds.	DPMO	95% Upper Bound (dpmo)	Z_{ST}
1	3900SM	19	52	1	5200	192	912	5.05
2	39001SM	34	44	1	4400	227	1078	5.01
3	39002SM	36	84	1	8400	119	565	5.17

Opportunities	3
TDU	5.386E-04
dpmo	180
Zst	5.07

Table 7

Analysis 6: Assumed mean is off centered with Monte Carlo Simulation

Scorecard: Method - Monte Carlo Simulation

Conditions: Assume mean is off centered at 0.002 in a 3-simga process with upper gap spec limit = 0.006

Note: Mean is approximated by 1/3*(Max - Min)

Probability of the number of unsoldered and/or poor lead connections for every 100 boards.

Line	P/N	# of Boards using socket	Socket Type	Defective	# of pins/100 bds.	DPMO	95% Upper Bound (dpmo)	Z_{ST}
1	3900SM	19	52	1	5200	192	912	5.05
2	39001SM	34	44	1	4400	227	1078	5.01
3	39002SM	36	84	1	8400	119	565	5.17

Opportunities	3
TDU	5.386E-04
dpmo	180
Zst	5.07

Table 8

Surface Mount Sockets Illustration- Without Monte Carlo Method

Assumptions: mean centered at 0.003 with a standard deviation 0f 0.001 in a 3-sigma process with upper gap spec limit = 0.006

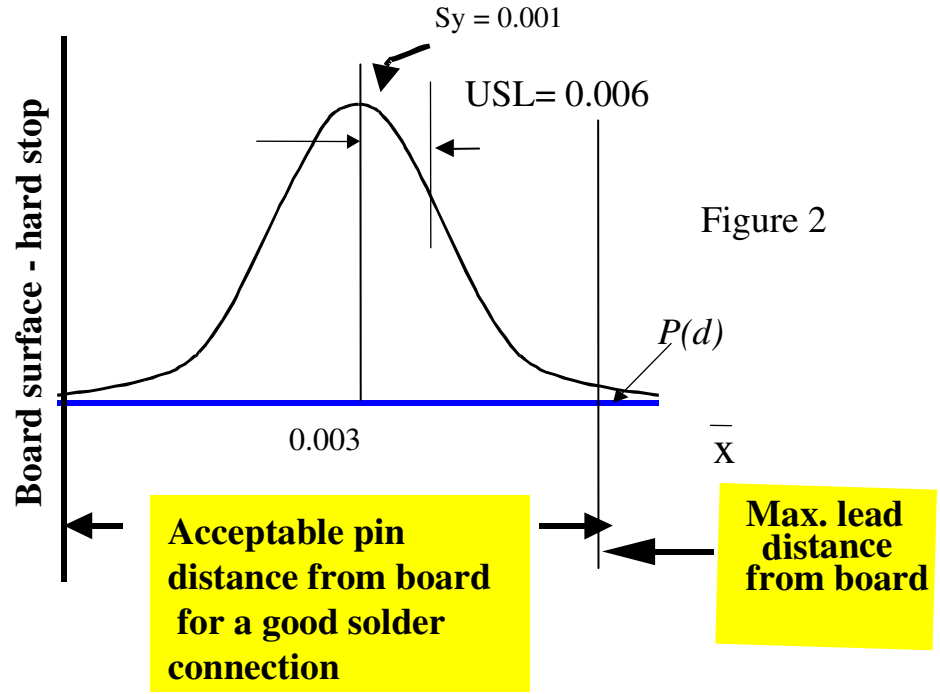

Figure 2

$$Estimated\ \ std.dev. = \frac{USL - 0}{6} = \frac{0.006 - 0}{6} = 0.001$$

$$\therefore z_{LT} = \frac{USL - 0.003}{s} = \frac{0.006 - 0.003}{0.001} = 3.0$$

$$z_{ST} = z_{LT} + z_{Shift} = 3.0 + 1.5 = 4.5$$

Probability of a gap being greater than 0.006 inch is 0.135%

Surface Mount Sockets Illustration- Monte Carlo Method

Input
Mean = 0.003
Std. Dev. = 0.001

Monte Carlo Method
sample 10,000 points
$Y=f(x_1,x_2)$

Output
Mean = 0.003043
Std. Dev. = 0.000984
Zst = 4.48

Input

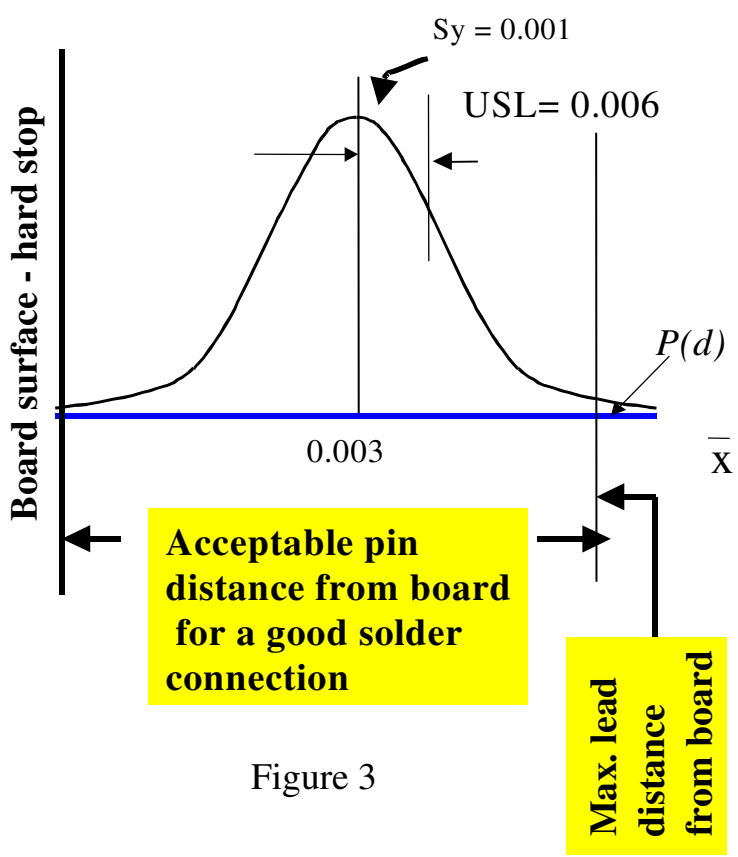

Figure 3

Output

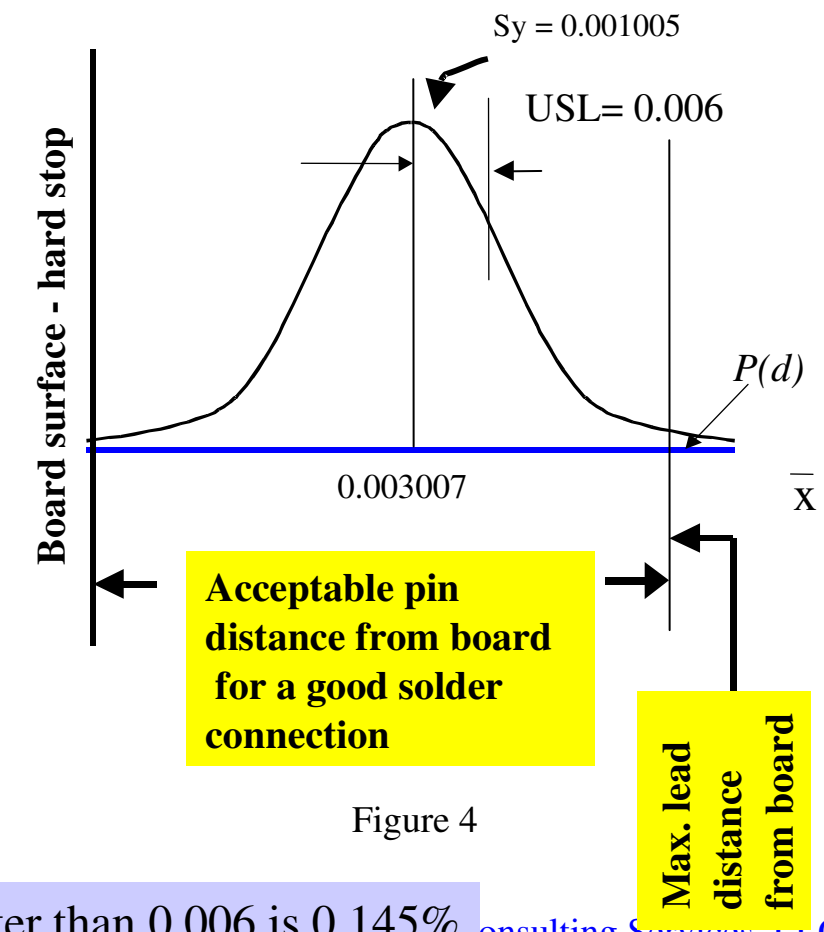

Figure 4

Probability of the gap being greater than 0.006 is 0.145%

Chi-Square distribution - count of unsoldered pins

Contingency Table

Expected counts are printed below observed counts

	Mean = 0.003	Mean = 0.004	Mean = 0.002	Total
Without Monte Carlo	25	409	3	437
	30.76	402.76	3.48	
With Monte Carlo	28	285	3	316
	22.24	291.24	2.52	
Total	53	694	6	753

Chi-Square = 1.078 + 0.097 + 0.067 + 1.491 + 0.134 + 0.092 = 2.958
DF = 2, P-Value = 0.228, 2 cells with expected counts less than 5.0